WEST

End of Result Set

Generate Collection Print

File: USPT

L1: Entry 1 of 1

US-PAT-NO: 6252305
DOCUMENT-IDENTIFIER: US 6252305 B1

TITLE: Multichip module having a stacked chip arrangement

DATE-ISSUED: June 26, 2001

INVENTOR-INFORMATION: NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chun Hung	Kaohsiung			TW
Chen; Kuang-Hui	Kaohsiung			TW
Wang; Shyh-Wei	Tainan			TW
Tao; Su	Kaohsiung			TW

US-CL-CURRENT: 257/777; 257/686, 257/723, 257/783, 257/784, 257/786

CLAIMS:

What is claimed is:

1. A multichip module comprising:

a substrate having a structure for making external electrical connection;

first, second, third and fourth semiconductor chips each consisting essentially of a single row of bonding pads formed on an active surface thereof and disposed on a side portion thereof, wherein

said first chip being attached to the substrate;

said second chip being attached to the active surface of the first chip such that the two respective rows of bonding pads on the first and second chips are substantially parallel and opposing to each other, and the side portion of the second chip having bonding pads formed thereon projects from the first chip;

said third chip being attached to the active surface of the second chip such that the row of bonding pads on the third chip is substantially perpendicular to the two rows of bonding pads on the first and second chips;

said fourth chip being attached to the active surface of the third chip such that the two rows of bonding pads on the third and fourth chips are substantially parallel and opposing to each other, and the side portion of the fourth chip having bonding pads formed thereon projects from the third chip; and

said third and fourth chips each have a width smaller than a perpendicular distance separating the two rows of bonding pads on the first and second chips; and

a plurality of bonding wires electrically connecting the bonding pads of each

chip to the structure for making external electrical connection.

2. A multichip module comprising:

a substrate having a structure for making external electrical connection;

first, second, third and fourth semiconductor chips each consisting essentially of a single row of bonding pads formed on an active surface thereof and disposed on a side portion thereof, wherein

said first chip being attached to the substrate;

said second chip being attached to the active surface of the first chip such that the row of bonding pads on the second chip is substantially perpendicular to the row of bonding pads on the first chip, and the side portion of the second chip having bonding pads formed thereon projects from the first chip;

said third chip being attached to the active surface of the second chip such that the row of bonding pads on the third chip is substantially perpendicular to the row of bonding pads on the second chip, and the side portion of the third chip having bonding pads formed thereon projects from the second chip;

said fourth chip being attached to the active surface of the third chip such that the row of bonding pads on the fourth chip is substantially perpendicular to the row of bonding pads on the third chip, and the side portion of the fourth chip having bonding pads formed thereon projects from the third chip; and

the second and fourth chips each having a width smaller than a perpendicular distance separating the two respective rows of bonding pads on the first and third chips; and

a plurality of bonding wires electrically connecting the bonding pads of each chips to the structure for making external electrical connection.

End of Result Set

Generate Collection | Print

L3: Entry 1 of 1 File: USPT

US-PAT-NO: 5998864
DOCUMENT-IDENTIFIER: US 5998864 A

TITLE: Stacking semiconductor devices, particularly memory chips

DATE-ISSUED: December 7, 1999

INVENTOR-INFORMATION: NAME	CITY	STATE	ZIP CODE	COUNTRY
Khandros; Igor Y.	Orinda	CA		
Pedersen; David V.	Scotts Valley	CA		

US-CL-CURRENT: 257/723; 257/668, 257/686, 257/691, 257/698, 257/724, 257/730, 257/731, 257/777, 257/778, 257/786, 361/735

CLAIMS:

What is claimed is:

1. A semiconductor package assembly, comprising:

an interconnection substrate having a plurality of terminals;

a first bare semiconductor device having a front surface and a back surface, and also comprising a plurality of terminals on the front surface;

a second bare semiconductor device stacked atop the first semiconductor device having a front surface and a back surface, and also comprising a plurality of terminals on the front surface,

each of the first and second bare semiconductor devices having a front surface and a back surface;

the second bare semiconductor device disposed in an offset stacked manner so that the front surface of the second bare semiconductor device is adjacent the back surface of the first bare semiconductor device, and an edge portion of the second bare semiconductor device is exposed beyond an edge of the first bare semiconductor device;

a first set of elongate interconnection elements extending from the terminals on the front surface of the first bare semiconductor device, said first set of elongate interconnection elements having free ends contacting a first portion of the plurality of terminals on the interconnection substrate; and

a second set of elongate interconnection elements extending from the terminals on the front surface of the second bare semiconductor device, said terminals disposed in the edge portion of the second bare semiconductor device, said second set of elongate interconnection elements having free ends contacting a second portion of the plurality of terminals on the interconnection substrate

wherein the terminals on the interconnection substrate are plated through holes.

2. The semiconductor package assembly, according to claim 1, wherein:

the second bare semiconductor device is offset in one direction from the first bare semiconductor device so that the edge portion is rectangular.

3. The semiconductor package assembly, according to claim 1, wherein:

the second bare semiconductor device is offset in two directions from the first bare semiconductor device so that the edge portion is L-shaped.

4. The semiconductor package assembly, according to claim 1, further comprising:

a third additional bare semiconductor device having a front surface and a back surface; and also comprising a plurality of terminals on the front surface,

the third bare semiconductor device disposed atop the second bare semiconductor device in an offset stacked manner so that the front surface of the third bare semiconductor device is adjacent the back surface of the second bare semiconductor device, and an edge portion of the third bare semiconductor device is exposed beyond an edge of the second bare semiconductor device;

a third set of elongate interconnection elements extending from the terminals on the front surface of the third bare semiconductor device, said terminals disposed in the edge portion of the third bare semiconductor device, said third set of elongate interconnection elements having free ends contacting a third portion of the plurality of terminals on the interconnection substrate.

5. The semiconductor package assembly, according to claim 1, wherein the first and second bare semiconductor devices comprise a first stacked subassembly, and further comprising:

a second stacked subassembly formed in the manner of the first stacked subassembly;

the elongate interconnection elements of the second stacked subassembly having free ends contacting a third portion of the plurality of terminals on the interconnection substrate and a fourth portion of the plurality of terminals on the interconnection substrate.

6. The semiconductor package assembly, according to claim 5, wherein the interconnection substrate has a front surface and a back surface; and wherein:

the first and second plurality of terminals on the interconnection substrate are disposed on the front surface of the interconnection substrate; and

the third plurality of terminals on the interconnection substrate are disposed on the front surface of the interconnection substrate.

7. The semiconductor package assembly, according to claim 5, wherein the interconnection substrate has a front surface and a back surface; and wherein:

the first and second plurality of terminals on the interconnection substrate are disposed on the front surface of the interconnection substrate; and

the third plurality of terminals on the interconnection substrate are disposed on the back surface of the interconnection substrate.

8. The semiconductor package assembly, according to claim 1, wherein:

the interconnection substrate is a printed circuit board.

9. The semiconductor package assembly, according to claim 1, wherein:

the semiconductor devices are memory chips.

10. The semiconductor package assembly, according to claim 1, wherein:

the elongate interconnection elements are resilient contact structures.

11. The semiconductor package assembly, according to claim 1, wherein:

selected ones of the terminals of at least one of the first and second bare semiconductor devices are re-routed from an initial location to a desired location on the semiconductor device.

12. The semiconductor package assembly, according to claim 1, further comprising:

a material selected from the group consisting of solder, braze and conductive epoxy securing the free ends of the interconnection elements to the terminals on the interconnection substrate.

13. A semiconductor package assembly, comprising:

an interconnection substrate having a plurality of terminals;

a first bare semiconductor die having a first surface facing the interconnection substrate and a second surface; and also comprising a plurality of terminals on the first surface;

a second bare semiconductor die having a first surface facing the interconnection substrate and a second surface, and stacked atop the first semiconductor die; and also comprising a plurality of terminals on the first surface;

the second bare semiconductor die disposed in an offset stacked manner so that the first surface of the second bare semiconductor die is adjacent the second surface of the first bare semiconductor die, and an edge portion of the second bare semiconductor die is exposed beyond an edge of the first bare semiconductor die;

a first set of elongate interconnection elements extending from the terminals on the first surface of the first bare semiconductor die, said first set of elongate interconnection elements having free ends contacting a first portion of the plurality of terminals on the interconnection substrate; and

a second set of elongate interconnection elements extending from the terminals on the first surface of the second bare semiconductor die, said terminals disposed in the edge portion of the second bare semiconductor die, said second set of elongate interconnection elements having free ends contacting a second portion of the plurality of terminals on the interconnection substrate

wherein the terminals on the interconnection substrate are plated through holes.

14. The semiconductor package assembly, according to claim 13, wherein:

the second bare semiconductor die is offset in at least one dimension so that the second bare semiconductor die extends beyond an edge of the first semiconductor die.

15. The semiconductor package assembly, according to claim 13, wherein the first and second bare semiconductor die comprise a first stacked subassembly, and further comprising:

a second stacked subassembly formed in the manner of the first stacked subassembly;

the elongate interconnection elements of the second stacked subassembly having free ends contacting a third portion of the plurality of terminals on the interconnection substrate and a fourth portion of the plurality of terminals on the interconnection substrate.

16. The semiconductor package assembly, according to claim 15, further comprising the interconnection substrate having a first surface and a second surface, and wherein:

the first stacked subassembly is disposed on the first surface of the substrate; and

the second stacked subassembly is disposed on the second surface of the substrate.

17. The semiconductor package assembly, according to claim 13, wherein:

the interconnection substrate is a printed circuit board.

18. The semiconductor package assembly, according to claim 13, wherein:

the semiconductor die are memory chips.

19. The semiconductor package assembly, according to claim 13, wherein:

the elongate interconnection elements are resilient contact structures.

20. The semiconductor package assembly, according to claim 13, wherein:

selected ones of the terminals of at least one of the first and second bare semiconductor devices are re-routed from an initial location to a desired location on the semiconductor device.

21. The semiconductor package assembly, according to claim 13, further comprising:

a material selected from the group consisting of solder, braze and conductive epoxy securing the free ends of the interconnection elements to the terminals on the interconnection substrate.

22. The semiconductor package assembly, comprising:

an interconnection substrate having a plurality of terminals;

a first bare semiconductor die having a first surface facing the interconnection substrate and a second surface; and also comprising a plurality of terminals on the first surface;

a second bare semiconductor die having a first surface facing the interconnection substrate and a second surface, and stacked atop the first semiconductor die; and also comprising a plurality of terminals on the first surface;

the second bare semiconductor die disposed in an offset stacked manner so that the first surface of the second bare semiconductor die is adjacent the second surface of the first bare semiconductor die, and an edge portion of the second bare semiconductor die is exposed beyond an edge of the first bare semiconductor die;

a first set of elongate interconnection elements extending from terminals on the first surface of the first bare semiconductor die, said first set of elongate interconnection elements having free ends directly in contact with a first portion of the plurality of terminals on the interconnection substrate; and

a second set of elongate interconnection elements extending from terminals on the first surface of the second bare semiconductor die, said terminals disposed in the edge portion of the second bare semiconductor die, said second set of elongate interconnection elements having free ends directly in contact with a second portion of the plurality of terminals on the interconnection substrate

wherein the terminals on the interconnection substrate are plated through holes.

23. The semiconductor package assembly, according to claim 22, wherein:

the second bare semiconductor die is offset in at least one dimension so that the second bare semiconductor die extends beyond an edge of the first semiconductor die.

24. The semiconductor package assembly, according to claim 22, wherein the first and second bare semiconductor dice comprise a first stacked subassembly, and further comprising:

a second stacked subassembly formed in the manner of the first stacked subassembly;

the elongate interconnection elements of the second stacked subassembly having free ends directly in contact with a third portion of the plurality of terminals on the interconnection substrate and a fourth portion of the plurality of terminals on the interconnection substrate.

25. The semiconductor package assembly, according to claim 24, further comprising the interconnection substrate having a first surface and a second surface, and wherein:

the first stacked subassembly is disposed on the first surface of the substrate; and

the second stacked subassembly is disposed on the second surface of the substrate.

26. The semiconductor package assembly, according to claim 22, wherein:

the interconnection substrate is a printed circuit board.

27. The semiconductor package assembly, according to claim 22, wherein:

the semiconductor devices are memory chips.

28. The semiconductor package assembly, according to claim 22, wherein:

the elongate interconnection elements are resilient contact structures.

29. The semiconductor package assembly, according to claim 22, wherein:

selected ones of the terminals of at least one of the first and second bare semiconductor devices are re-routed from an initial location to a desired location on the semiconductor device.

30. The semiconductor package assembly, according to claim 22, further comprising:

a material selected from the group consisting of solder, braze and conductive epoxy securing the free ends of the interconnection elements to the terminals on the interconnection substrate.